Monday afternoon session introduction

PRETSY
Precision-Timed Synchronous Reactive Processing

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SYNCHRON 2011, Le Bois du Lys
PRETSY — Overview

What we can build on

Project Agenda
PRETSY — Overview

- **Objective:** Establish holistic approach for the design of timing-predictable, efficient reactive systems
- Synchronous model of computation
  - $\Rightarrow$ analyzability at language level
- PRET-like architecture
  - $\Rightarrow$ analyzability at architecture level
- Three-year project (German Science Foundation)
What we can build on

Languages:
- Esterel, Lustre, Signal, SyncCharts, Lucid Synchrone ...
- Lusterel (Bamberg/Paris)
- PRET-C (Auckland/Grenoble), Synchronous C/J (Kiel)
  → talk by R. v. Hanxleden

Analyses/Compilation:
- WCET analysis (Saarbrücken, ...)  
  → talks by R. Wilhelm, V. Rodrigues
- WCRT analysis (Bamberg, Kiel, Auckland, Grenoble) 
  → talks by P. Roop, R. v. Hanxleden
- Large body of work on synchronous compilation

Architectures:
- REMIC, REPIC, Emperor, StarPro (Auckland), KEP/KLEP (Kiel)
- PRET (Berkeley/Columbia), ARPRET (Auckland)
Project Agenda

Languages:
- Mixed-style synchronous modeling language + host language
- Semantics to be formalized and implemented in Haskell

Analyses/Compilation:
- Heuristics based on compositional WCRT interface algebra → talk by M. Mendler
- Synthesis/analysis path between modeling language and architecture that preserves timing

Architectures:
- PRET with efficient support for synchronous reactive control flow
- Classic ISA + reactive/scheduling instructions

Thanks!