HELP: High-Level Models For Low-Power HW/SW Systems

The HELP people, among which, for today’s talk:
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Verimag

SYNCHRON’11 Le Bois du Lys
1. Context

2. The HELP Generic Modeling Principles

3. A Question Related to the Discrete/Continuous Parts

4. Ongoing Work
Context: The HELP Project 2009-2012

- Verimag/Synchrone (Florence, Matthieu Moy, Tayeb Bouhadiba, Claire Maiza, Catherine Parent)
- INRIA AOSTE (Robert, ...)
- LEAT Nice
- STMicroelectronics Grenoble
- DOCEA Power Grenoble

Provide early evaluations of energy consumption for systems-on-a-chip, at the transactional level (TLM).
Systems on a Chip
Systems on a Chip

On a processor:
- A real-time OS + several processes
- Hardware IP’s (components)
Transaction-Level Modeling

RTL
Synthesizable+
Cycle and Data Accurate+
Slow Simulations−
Transaction-Level Modeling

TLM
+ Early Available
+ Fast Simulations
− Not synthesizable

RTL
Synthesizable+
Cycle and Data Accurate+
Slow Simulations−
Sources of Energy Consumption and Available Mechanisms for Reducing It

Sources:
- Static, leakage currents (indep. of the behavior)
- Dynamic, when transistors commute (related to the behavior)

Solutions for reducing energy consumption:
Sources of Energy Consumption and Available Mechanisms for Reducing It

Sources:
- Static, leakage currents (indep. of the behavior)
- Dynamic, when transistors commute (related to the behavior)

Solutions for reducing energy consumption:
Do not build systems-on-a-chip!
Sources of Energy Consumption and Available Mechanisms for Reducing It

Sources:
- Static, leakage currents (indep. of the behavior)
- Dynamic, when transistors commute (related to the behavior)

Solutions for reducing energy consumption:
- Clock gating
- Power gating
- Dynamic Voltage and Frequency Scaling (DVFS)
Low Power SoC Design Solutions

Most of these are defined in the Unified Power Format (UPF).
Low Power SoC Design Solutions

- Clock Gating
  - Save Dynamic Power

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SoC

clk

enable

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Most of these are defined in the Unified Power Format (UPF).

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Low Power SoC Design Solutions

- Clock Gating
  - Save Dynamic Power
- Multi-VDD

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Low Power SoC Design Solutions

- Clock Gating
  - Save Dynamic Power
- Multi-VDD
  - Needs Level Shifters

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Low Power SoC Design Solutions

- Clock Gating
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Low Power SoC Design Solutions

- Clock Gating
  - Save Dynamic Power
- Multi-VDD
  - Needs Level Shifters
- Power Gating
  - Save static power
  - Needs isolation

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Low Power SoC Design Solutions

- **Clock Gating**
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- **Multi-VDD**
  - Needs Level Shifters
- **Power Gating**
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  - Needs isolation
  - (May) needs retention

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Low Power SoC Design Solutions

- **Clock Gating**
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Most of these are defined in the Unified Power Format (UPF)
Power Domains (picture by Ons Mbarek, LEAT)
Power Management Policies

A power management policy = a strategy for reducing energy, playing with clock/power gating and DVFS, based on observations: temperature sensor, “functional sensors” (contents of a FIFO), ... 

Implementations: HW/SW, Centralized/distributed, ... 

Complex feedback effect, need for virtual protoyping (= playing the SW on a model of the HW + Φ).
Existing Evaluation Tools

- At the gate or register-transfer (RT) levels: industrial tools, precise but very slow
- At the transaction level: several proposals for specific components (bus, network on chip, processors, ...) but nothing for a system-wide model integrating the SW
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Example System

- CPU
- RAM
- Display
- MPEG decoder
Example System

Action on power modes

- CPU
- RAM
- Display
- MPEG decoder
- Power Controller
Example System

- Temperature Sensor
- Action on power modes
- Power Controller
- RAM
- MPEG decoder
- CPU
- Display

Action on power modes:
- Power Controller
- Temperature Sensor
- MPEG decoder
- RAM
- Display
- sw
Example System

- **Heat Feedback loop**
  - Power Controller
  - Temperature Sensor
  - Action on power modes
- **Components**
  - Display
  - MPEG decoder
  - RAM
  - Switch (sw)
- **Actions**
  - Heat

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The HELP Approach

- Gather information on the consumption of components (as power-state models)
- Build a Transaction-level model of the SoC, and simulate it, including the SW
Power-State Models

\[
\begin{align*}
A & \xrightarrow{-a} -a \\
& \xleftarrow{a} A \\
B[3t] & \xrightarrow{b} B[3t] \\
& \xleftarrow{b} B[3t] \\
C[2t] & \xrightarrow{-a} C[2t] \\
& \xleftarrow{a} C[2t]
\end{align*}
\]

ext. input

time [x units]

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Power-State Models

\[ \frac{d}{dt} \]

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Power-State Models

\[ \frac{de}{dt} \]

\[ a \]

\[ b \]

\[ -a \]

Time [x units]

Ext. Input

C[2t]

B[3t]

A

5

20

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Power-State Models

\[ \text{time [x units]} \]
\[ \text{ext. input} \]
\[ \frac{d}{dt} \]

\begin{align*}
A & \quad 5 \\
C[2t] & \quad 20 \\
B[3t] & \quad 2
\end{align*}

\[ \text{time t} \]
Power-State Models

\[ \frac{de}{dt} = a \]

Time [\( x \) units]
ed \( \frac{de}{dt} \)

Ext. input

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Power-State Models

A

5

B[3t]

2

C[2t]

20

de/dt

ext. input

-a

a

b

-b

-A

5 5

B 2 17

C 20 41

B 2 21

C 20 61

B 2 63

A 5 70

Cumulated consumption

time t

time [x units]
Modeling Time (when not cycle-accurate)

Active part (thread) in the model of a component:

...  
f() ; // do some functional  
     // effect locally  
wait ([T1,T2]) ; // pretend it takes some time  
port.write (...); // communicate with another  
     // component by  
     // initiating a transaction  
...
The HELP Generic Modeling Principles (1)
The HELP Generic Modeling Principles (1)
The HELP Generic Modeling Principles (1)
Brown: the functional and approximate time TLM model of the chip, able to run the real software.

Green: one “consumption automaton” per component, describing the current state of operation. The states of these automata are driven by the power manager actions. Examples:

- retention mode for the RAM
- several low-power modes for the CPU
- ON/OFF for the display
- ...

The HELP Generic Modeling Principles
The HELP Generic Modeling Principles (2)
The HELP Generic Modeling Principles (2)

- **Brown**: the functional+time TLM model of the chip, able to run the real software.
- **Green**: one “consumption automaton” per component
- **Purple**: another consumption automaton per component, whose states are driven by the functional+time part. Example: the LCD display.
“Purple” consumption automaton for the LCD

Displaying one line

- Carriage return
- Corner delay
- Return to top left
The HELP Generic Modeling Principles (3)
The HELP Generic Modeling Principles (3)

Temperature Sensor
Power Controller
Display
MPEG decoder
RAM
SW
U

High
Low

?
The HELP Generic Modeling Principles (3)

- **Brown**: the functional+time TLM model of the chip, able to run the real software.
- **Green**: one “consumption automaton” per component
- **Purple**: another consumption automaton per component
- **Pink**: yet another consumption automaton per component, whose states are driven by the *traffic*. Example: the bus
“Pink” consumption automaton for the Bus

For the bus, deducing the current consumption state from the functional behavior requires a very detailed functional model.

The significant consumption states are known from measures on existing busses, and can be related to the traffic.

In the model, the “Pink” consumption automaton is driven by an observation of the traffic (the input/output ports of the component).
The HELP Generic Modeling Principles (4)
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Discrete/Continuous Parts

Discrete consumption

Continuous

Temp = \( F \) (Consumption)

Tools:
DOCEA Aceplorer
ATMI
HotSpot
## Discrete/Continuous Parts

<table>
<thead>
<tr>
<th>Discrete consumption</th>
<th>Continuous</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Discrete Consumption Diagram" /></td>
<td>Temp = F (Consumption)</td>
</tr>
</tbody>
</table>

**Model in a synchronous language**
A Question Related to the Discrete/Continuous Parts

Discrete/Continuous Parts

Discrete consumption

Model in a discrete–event modeling language.

Continuous

\[ \text{Temp} = F(\text{Consumption}) \]

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A Question Related to the Discrete/Continuous Parts

Discrete/Continuous Parts

Discrete consumption

Model in a discrete–event modeling language.

Continuous

Temp = F (Consumption)

Temp at tj
(for the temp sensor)
Temperature Model

Floorplan of the SoC

CPU  MEM
LCD  Temp
DMA  BUS
Temperature Model

Floorplan of the SoC
Temperature Model

Floorplan of the SoC

Electrical View of Temperature Propagation

CPU
MEM
LCD
DMA
Temp
BUS
1. Context

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4. Ongoing Work
Ongoing Work

- Decisions on *when* to switch between the two parts
- Formalization of the traces and errors that occur when “sampling” is slow
- Technical work on the connection (with thrift) between SystemC/TLM & DOCEA Aceplorer
- *Case study: comparison with measures on the real system*